



# 21152 PCI-to-PCI Bridge Configuration

Application Note

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## 1.0 Introduction

This application note describes the configuration of the 21152 PCI-to-PCI bridge chip in a system. This application note is limited to the PCI configuration of the 21152 only and does not cover any hardware application topics, or describe the details of the PCI protocol.

The following topics are included in this document:

- Summary of the 21152 configuration space
- Default state of the 21152 configuration space
- Initialization guidelines for the 21152
- Sample initializations

## 2.0 Functional Overview

The 21152 PCI-to-PCI Bridge connects two independent PCI buses. You can implement the 21152 either on a system motherboard or backplane to provide capability for additional slots and devices, or on an option card to allow for multiple devices. You can also use the 21152 to isolate bus traffic and to provide concurrent primary and secondary bus operation.

The 21152 is a transparent device; that is, it requires no special driver software to run in a system. The 21152 does require initialization code to set up its configuration space, allocate memory and I/O space on the secondary bus of the 21152, and identify VGA devices behind the 21152. This initialization code resides in the system BIOS code or system firmware.

Once configured, the 21152 operates without the need for any additional software control.

## 3.0 21152 Configuration Space

The configuration registers of the 21152 comply with the registers of the type 1 configuration header format for PCI-to-PCI bridges, as specified in the *PCI-to-PCI Bridge Architecture Specification*. The first 16 bytes of this header are identical to those of any other PCI device. The remaining 48 bytes of the predefined header are specific to the PCI-to-PCI bridge architectural standard. The 21152 also implements 12 bytes of implementation-specific configuration space header. For a detailed description of each field, see the *21152 PCI-to-PCI Bridge Data Sheet*.

Figure 1 shows a configuration space map for the 21152.

**Figure 1. 21152 Configuration Space Map**

31

16 15

00

Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h
Reserved				14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32 Bits				28h
Prefetchable Memory Limit Address Upper 32 Bits				2Ch
I/O Limit Address Upper 16 Bits		I/O Base Address Upper 16 Bits		30h
Reserved*			ECP Pointer*	34h
Reserved				38h
Bridge Control		Interrupt Pin	Reserved	3Ch
Arbiter Control		Diagnostic Control	Chip Control	40h
Reserved				44h
Reserved				48h
Reserved				4Ch
Reserved				50h
Reserved				54h
Reserved				58h
Reserved				5Ch
Reserved				60h
Reserved	Reserved	Reserved	p_serr_I Event Disable	64h
Reserved	p_serr_I Status	Secondary Clock Control		68h
Reserved				6Ch - DBh
Power Management Capabilities**		Next Item Ptr**	Capability ID**	DCh
Data	PMCSR Bridge Support Extensions**	Power Management CSR**		E0h
Reserved				E4h - FFh

\* 21152-AB only; in the 21152-AA, these registers are R/W Subsystem ID and Subsystem Vendor ID.

\*\* These are reserved for the 21152-AA.

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The following tables provide the bit definitions of 21152 control and status registers. For a description of these bits, see the *21152 PCI-to-PCI Bridge Data Sheet*.

**Table 1. Primary Command Register**

Primary Command - Offset 04h (Dword Address 04h)		
Field Bit	Dword Bit	Description
0	0	I/O space enable
1	1	Memory space enable
2	2	Master enable
3	3	Special cycle enable
4	4	Memory write and invalidate enable
5	5	VGA snoop enable
6	6	Parity error response
7	7	Wait cycle control
8	8	SERR# enable
9	9	Fast back-to-back enable
15:10	15:10	Reserved

**Table 2. Primary Status Register**

Primary Command - Offset 06h (Dword Address 04h)		
Field Bit	Dword Bit	Description
3:0	19:16	Reserved
4	20	ECP enable <sup>1</sup>
5	21	66-MHz capable
6	22	Reserved
7	23	Fast back-to-back capable
8	24	Data parity detected
10:9	26:25	Primary DEVSEL# timing
11	27	Signaled target abort
12	28	Received target abort
13	29	Received master abort
14	30	Signaled system error
15	31	Detected parity error

1. 21152-AB and later revisions only. These registers are reserved in 21152-AA.

**Table 3. Secondary Status Register**

Secondary Status - Offset 1Eh (Dword Address 1Ch)		
Field Bit	Dword Bit	Description
4:0	20:16	Reserved
5	21	66-MHz capable
6	22	Reserved
7	23	Fast back-to-back capable
8	24	Data parity detected
10:9	26:25	s_devsel_I timing
11	27	Signaled target abort
12	28	Received target abort
13	29	Received master abort
14	30	Received detected system error
15	31	Detected parity error

**Table 4. Bridge Control Register**

Bridge Control-Offset 3Eh (Dword Address 3Ch)		
Field Bit	Dword Bit	Description
0	16	Parity error response
1	17	SERR# forward enable
2	18	ISA enable
3	19	VGA enable
4	20	Reserved
5	21	Master abort mode
6	22	Secondary bus reset
7	23	Fast back-to-back control
8	24	Primary master timeout
9	25	Secondary master timeout
10	26	Master timeout status
11	27	Master timeout SERR# enable
15:10	31:28	Reserved



**Table 5. Chip Control-Offset 3Eh (Dword Address 3Ch)**

Chip Control-Offset 40h (Dword Address 40h)		
Field Bit	Dword Bit	Description
0	0	Reserved
1	1	Memory write disconnect control
3:2	3:2	Reserved
4	4	Secondary bus prefetch disable
7:5	7:5	Reserved

**Table 6. Diagnostic Control Register**

Diagnostic Control-Offset 41h (Dword Address 40h)		
Field Bit	Dword Bit	Description
0	8	Chip reset
2:1	10:9	Test mode
7:3	15:11	Reserved

**Table 7. Arbiter Control Register**

Arbiter Control-Offset 42h (Dword Address 40h)		
Field Bit	Dword Bit	Description
10:0	25:16	Arbiter control
15:11	31:26	Reserved

**Table 8. p\_serr\_I Event Disable Register**

p_serr_I Event Disable -Offset 64h (Dword Address 64h)		
Field Bit	Dword Bit	Description
0	0	Reserved
1	1	Posted write parity error
2	2	Posted write nondelivery
3	3	Target abort during posted write
4	4	Master abort on posted write
5	5	Delayed write nondelivery
6	6	Delayed read?no data from target
7	7	Reserved

**Table 9. Secondary Clock Control Register**

Secondary Clock Control-Offset 68h (Dword Address 68h)		
Field Bit	Dword Bit	Description
1:0	1:0	Clock 0 disable
3:2	3:2	Clock 1 disable
5:4	5:4	Clock 2 disable
7:6	7:6	Clock 3 disable
8	8	Clock 4 disable
15:5	15:5	Reserved

**Table 10. p\_serr\_I Status Register**

p_serr_I Status-Offset 6Ah (Dword Address 68h)		
Field Bit	Dword Bit	Description
0	16	Address parity error
1	17	Posted write data parity error
2	18	Posted write nondelivery
3	19	Target abort during posted write
4	20	Master abort during posted write
5	21	Delayed write nondelivery
6	22	Delayed read—no data from target
7	23	Delayed transaction master timeout

**Table 11. Power Management Capabilities Register<sup>1</sup>**

Power Management Capabilities-Offset DEh (Dword Address DCh)		
Field Bit	Dword Bit	Description
2:0	18:16	Power management revision
3	19	PME# clock required
4	20	Auxiliary power support
5	21	Device-specific initialization
8:6	24:22	Reserved
9	25	D1 support
10	26	D2 support
15:11	31:27	PME# support

1. 21152-AB only. These registers are reserved in the 21152-AA.

**Table 12. Power Management Control and Status Register<sup>1</sup>**

Power Management Control and Status-Offset E0h (Dword Address E0h)		
Field Bit	Dword Bit	Description
1:0	1:0	Power state
7:2	7:2	Reserved
8	8	PME# enable
12:9	12:9	Data select
14:13	14:13	Data scale
15	15	PME# status

1. 21152-AB only. These registers are reserved in the 21152-AA.

**Table 13. PPB Support Extensions Register<sup>1</sup>**

PPB Support Extensions-Offset E2h (Dword Address ECh)		
Field Bit	Dword Bit	Description
5:0	21:16	Reserved
6	22	B2_B3 support
7	23	Bus power/clock control enable

1. 21152-AB only. These registers are reserved in the 21152-AA.

## 4.0 21152 Initial Conditions

After system reset, the 21152 is initialized to the following state:

- Memory, I/O, and master enables all reset to zero (disabled). The 21152 does not respond to any memory or I/O transactions on either the primary or secondary bus.
- Primary, secondary, and subordinate bus numbers are all reset to zero. You must initialize these bus numbers before you can configure any devices downstream of the 21152.
- Prefetchable memory, nonprefetchable memory, and I/O base and limit address registers are all zero. This does not mean that these address ranges are turned off. In fact, a memory range of addresses 000FFFFF (hex) - 00000000 (hex) and an I/O range of addresses 0FFF (hex) - 0000 (hex) are defined for downstream forwarding. Because the enables are off, no memory or I/O transactions are forwarded, however. Before turning on those enables, initialize these address ranges. To turn off downstream forwarding, set the address base to a value greater than the address limit.
- The primary and secondary master latency timers are set to zero. The 21152 will relinquish the bus after the first data transfer when the 21152's primary bus grant has been deasserted. The single exception is Memory Write and Invalidate (MWI) transactions.
- Cache line size is set to zero. No cache line boundaries are observed, and memory write and invalidate commands are forwarded as memory write commands.
- Parity checking, **p\_serr\_1** assertion, VGA modes, and ISA modes are all disabled.
- All device-specific features are disabled (reset to 0).

## 4.1 Configuration Register Values After Reset

Table 14 lists the value of the 21152 configuration registers after reset. Reserved registers are not listed and are always read as zero.

**Table 14. Configuration Register Values After Reset (Sheet 1 of 2)**

Byte Address	Register Name	Reset Value
00-01h	Vendor ID	1011h
02-03h	Device ID	0024h
04-05h	Command	0000h
06-07h	Status	0280h <sup>1</sup> 0290h <sup>2</sup>
08h	Revision ID	Initially 00h <sup>3</sup>
09-0Bh	Class code	060400h
0Ch	Cache line	00h
0Dh	Primary master latency timer	00h
0Eh	Header type	01h
18h	Primary bus number	00h

Table 14. Configuration Register Values After Reset (Sheet 2 of 2)

Byte Address	Register Name	Reset Value
19h	Secondary bus number	00h
1Ah	Subordinate bus number	00h
1Bh	Secondary master latency timer	00h
1Ch	I/O base	01h
1Dh	I/O limit	01h
1E-1Fh	Secondary status	0280h
20-21h	Memory-mapped I/O base	0000h
22-23h	Memory-mapped I/O limit	0000h
24-25h	Prefetchable memory base	0001h
26-27h	Prefetchable memory limit	0001h
28-2Bh	Prefetchable memory base upper 32 bits	00000000h
2C-2Fh	Prefetchable memory limit upper 32 bits	00000000h
30-31h	I/O base upper 16 bits	0000h
32-33h	I/O limit upper 16 bits	0000h
34-35h <sup>1</sup>	Subsystem Vendor ID	0000h
34h <sup>2</sup>	ECP pointer	DCh
35-37h <sup>2</sup>	Reserved	000000h
36-37h <sup>1</sup>	Subsystem ID	0000h
3Dh	Interrupt pin	00h
3E-3Fh	Bridge control	0000h
40h	Chip control	00h
41h	Diagnostic control	00h
42-43h	Arbiter control	0200h
64h	<b>p_serr_l</b> event disable	00h
68-69h	Secondary clock control	00h
6Ah	<b>p_serr_l</b> status	00h
DCh <sup>2</sup>	Power management capability ID	01h
DDh <sup>2</sup>	Next item	00h
DE-DFh <sup>2</sup>	Power management capabilities	0001h
E0-E1h <sup>2</sup>	Power management CSR	0000h
E2h <sup>2</sup>	PPB support extensions	xx000000b <sup>4</sup>
E3h <sup>2</sup>	Data register	00h

1. 21152-AA only.
2. 21152-AB and later revisions.
3. Dependent on revision of device. The first revision is read as 00h; subsequent revisions increment by 1.
4. Reset value dependent on state of **bpcc** pin.

## 4.2 Arbiter Values After Reset

After reset, the 21152 is initialized to the following state:

- All external masters are assigned to the low priority group, and the 21152 is assigned to the high priority group. The 21152 receives highest priority on the target bus every other transaction, and priority rotates evenly among the other masters.
- The 21152 parks the secondary bus at itself until transactions start occurring on the secondary bus. After a transaction has occurred, the secondary bus is parked at the last master to use the bus. If the internal arbiter is disabled, the 21152 parks the secondary bus only when the reconfigured grant signal, `s_req_l<0>`, is asserted and the secondary bus is idle.

## 5.0 System Initialization

The *PCI-to-PCI Bridge Architecture Specification* provides guidelines for initialization. Some of this information is included here to aid initialization code development.

When the 21152 or any other PCI-to-PCI bridge is present in a system, either on the system board or on a PCI option card, system BIOS or system firmware is required to provide the following functions during the initialization process:

- Assigning PCI bus numbers
- Allocating address ranges (prefetchable memory, nonprefetchable memory, and I/O)
- Writing the interrupt request (IRQ) number into each device
- Initializing the PCI display subsystem (if present)

## 6.0 Assigning PCI Bus Numbers

The system BIOS must assign PCI bus numbers to each PCI-to-PCI bridge in the system. The order and when the PCI bus numbers are assigned is not specified.

The following requirements must be followed:

- All buses located downstream of a PCI-to-PCI bridge must reside between the secondary bus number and the subordinate bus number (inclusive).
- Bus number ranges in parallel branches of PCI bus hierarchy must be mutually exclusive.

## 7.0 Allocating Address Ranges

The system BIOS must map all devices residing behind the bridge into one of the 21152 address ranges. Address ranges supported by the 21152 are I/O space, prefetchable memory, and nonprefetchable memory (also called memory-mapped I/O). The address ranges have the characteristics shown in Table 15.

**Table 15. Characteristics of Address Ranges**

Address Range	Maximum Range	Minimum Granularity
I/O	2 <sup>32</sup> Bytes (4GB)	4KB
Prefetchable memory	2 <sup>64</sup> Bytes	1MB
Nonprefetchable memory (memory-mapped I/O)	2 <sup>32</sup> Bytes (4GB)	1MB

## 8.0 Mapping I/O Space Using ISA Mode

When an ISA or EISA bus is in the system, I/O space can become fragmented. An ISA address uses only 10 bits of addressing, giving a maximum 1KB of address space. Because ISA devices decode only the lowest 10 bits, these addresses are aliased throughout the entire I/O space.

The bottom 256 bytes of a 1KB chunk point to system-specific addresses. The top 768 bytes are used for general I/O. EISA systems use the entire 64KB space by dividing the space into 16 4KB slots, and use a slot-specific control strobe to point to a particular slot. Slot 0 is generally allocated to the motherboard.

PCI-to-ISA and PCI-to-EISA bridges typically perform full 32-bit addressing, using positive decoding for the bottom 256 bytes of the first 1K chunk and subtractive decoding for the upper 768 bytes of each 1K chunk. Although the top 768 bytes of each chunk might be used for general ISA/EISA devices, the bottom 256 bytes in all slots except for slot 0 (the bottom 4K slots) are available for use by PCI devices.

The 21152 provides a mode that allows mapping into the low 256 bytes of each 1K chunk. When the ISA mode bit is set, the 21152 forwards only downstream transactions addressing the low 256 bytes of each 1K chunk inside the defined address range. This allows mapping of PCI devices into I/O space when there is an ISA or EISA bus in the system. When mapping a device downstream of the 21152 with ISA mode set, bits <9:8> of the device's I/O base address should be 00.

## 9.0 Using the 21152 VGA Modes

The 21152 can be configured to support VGA-compatible devices.

When a VGA-compatible device is located downstream of a PCI-to-PCI bridge, set the VGA mode bit in 21152 configuration space in every PCI-to-PCI bridge between the VGA device and the most primary PCI bus. Setting this bit configures the 21152 to pass all VGA frame buffer memory addresses and all VGA I/O addresses downstream.

When a graphics device that does not have VGA-compatibility is located downstream of the 21152, you must configure the bridge to forward only VGA palette writes by setting the VGA snoop bit in the 21152 configuration space. This bit must be set in every PCI-to-PCI bridge between the most primary PCI bus and the graphics device.

If both types of devices are located downstream of the 21152, setting the VGA mode bit is sufficient for proper operation. Setting both the VGA mode and the VGA snoop bits results in the same behavior as setting only the VGA mode bit.

For more information about VGA support in PCI systems, refer to the *PCI-to-PCI Bridge Architecture Specification*.

## 10.0 Sample 21152 Initializations

This section provides several sample initializations of the 21152.

### 10.1 Initializing the 21152 for Hierarchical Configuration Accesses

To initialize the 21152 so that configuration transactions can be forwarded, use the values in Table 16 to write the following bridge configuration registers (values in hex):

**Table 16. Bridge Configuration Register Values**

Dword Offset	Register	Value	Notes
04h	Primary status/ command	FFFF0000h	Clear all status bits. Make sure memory, I/O, and master enables are turned off.
18h	Subordinate/ secondary/primary	00xyzzh	xx = subordinate bus number yy = secondary bus number zz = primary bus number

The important points are:

- Turn off memory, I/O, and master enables to prevent memory and I/O transactions from crossing the bridge.
- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.



## 10.2 Initializing the 21152 for I/O and Configuration Forwarding

To initialize the 21152 so that I/O and configuration transactions can be forwarded, use the values in Table 17 to write the following bridge configuration registers (values in hex):

**Table 17. I/O and Configuration Transaction Values**

Dword Offset	Register	Value	Notes
18h	Subordinate/ secondary/ primary bus numbers	00xyyzzh	xx = subordinate bus number xy = secondary bus number zz = primary bus number
1Ch	Secondary status/ I/O limit address/ I/O base address	FFFFx0y0h	Clear status bits. x = I/O limit address bits <15:12> y = I/O base address bits <15:12>
20h	Memory limit/ memory base	0000FFFFh	Turn off downstream memory address range.
24h	PF memory limit/ PF memory base	0000FFFFh	Turn off downstream PF memory address range.
3Ch	Bridge control	000x0000h	x = 0 (no ISA bus in system) x = 4 (ISA bus in system)
04h	Primary status/command	FFFF0005h	Clear status bits. Turn on I/O enable for downstream I/O. Turn on master enable for upstream I/O. <b>Write this register last.</b>

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Initialize I/O base and limit registers to define a downstream window.
- Turn off both memory ranges.
- If an (E)ISA bus is in the system, turn on ISA mode.
- Turn on I/O and master enables. **Write this register last.**

**Note:** Setting the master enable bit also enables forwarding of the memory transactions upstream.

## 10.3 Initializing the 21152 for Memory and Configuration Forwarding

To initialize the 21152 so that memory and configuration transactions can be forwarded, use the values in Table 18 to write the following bridge configuration registers (values in hex):

**Table 18. Memory and Configuration Transactions**

Dword Offset	Register	Value	Notes
18h	Subordinate/ secondary/ primary bus numbers	00xyyzzh	xx = subordinate bus number yy = secondary bus number zz = primary bus number
1Ch	Secondary status/ I/O limit address/ I/O base address	FFFF00FFh	Clear status bits. Turn off I/O address range.
20h	Memory limit/ memory base	xxx0yyy0h	xxx = nonprefetchable memory limit address <31:20> yyy = nonprefetchable memory base address <31:20>
24h	PF memory limit/ PF memory base	xxx0yyy0h	xxx = prefetchable memory limit address <31:20> yyy = prefetchable memory base address <31:20>
04h	Primary status/ command	FFFF0006h	Clear status bits. Turn on memory enable for downstream memory. Turn on master enable for upstream memory. <b>Write this register last.</b>

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Turn off I/O range.
- Initialize either or both nonprefetchable and prefetchable memory ranges.
- Turn on memory and master enables. **Write this register last.**

**Note:** Setting the master enable bit also enables forwarding of the I/O transactions upstream.

## 10.4 Initializing the 21152 for Memory, I/O, and Configuration Forwarding

To initialize the 21152 so that memory, I/O, and configuration transactions can be forwarded, use the values in Table 19 to write the following bridge configuration registers (values in hex):

**Table 19. Memory, I/O, and Configuration Transactions**

Dword Offset	Register	Value	Notes
18h	Subordinate/secondary/primary bus numbers	00xyyyzzh	xx = subordinate bus number yy = secondary bus number zz = primary bus number
1Ch	Secondary status/I/O limit address/I/O base address	FFFFx0y0h	Clear status bits. x = I/O limit address bits <15:12> y = I/O base address bits <15:12>
20h	Memory limit/memory base	xxx0yyy0h	xxx = nonprefetchable memory limit address <31:20> yyy = nonprefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
24h	PF memory limit/PF memory base	xxx0yyy0h	xxx = prefetchable memory limit address <31:20> yyy = prefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
3Ch	Bridge control	000x0000h	x = 0 (no ISA bus in system) x = 4 (ISA bus in system)
04h	Primary status/command	FFFF0007h	Clear status bits. Turn on I/O enable for downstream I/O. Turn on memory enable for downstream memory. Turn on master enable for upstream memory and I/O. <b>Write this register last.</b>

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Initialize the I/O range.
- Initialize either or both nonprefetchable and prefetchable memory ranges.
- Turn on memory and master enables. **Write this register last.**

## 11.0 Initializing VGA Modes in the 21152

The following sections provide examples of initializing VGA mode and VGA snoop mode.

### 11.1 VGA Mode

If a VGA device resides behind the 21152, enable VGA mode. To enable VGA mode, write bit 18 of configuration address 3Ch. Simply modify the contents of the write to this register shown in previous sections. For example:

Dword Offset	Register	Value	Notes
3Ch	Bridge control	000x0000h	x = 8 (VGA mode; no ISA bus in system) x = C (VGA mode; ISA bus in system)

You must write this register before memory, I/O, and master enables located at configuration address 04h are set.

### 11.2 VGA Snoop Mode

If a graphics device requiring VGA snoop mode resides behind the 21152, you must write bit 5 of configuration address 04h. Simply modify the contents of the write to this register shown in previous sections. For example:

Dword Offset	Register	Value	Notes
04h	Primary status/command	FFFF002xh	x = 7 (Set memory, I/O, and master enable, if all memory and I/O ranges are used) x = 5 (Set I/O and master enable, if only the I/O range is used)

## 12.0 Initializing Optional Registers in the 21152

This section describes initialization of optional 21152 features. The features are not required for basic bridge operation. It is recommended that you write these registers before (or in the same access as) setting the memory, I/O, and master enables in configuration address 04h. Otherwise, order is not important.

### 12.1 Enabling Parity and Checking Errors

Table 20 lists the accesses to enable parity checking on both interfaces and to forward **seerr#** from the secondary to the primary interface.

**Table 20. Enabling Parity and Checking Errors**

Dword Offset	Register	Value	Notes
3Ch	Bridge control	000x0000h	x = 3 (No ISA bus in system, no VGA behind 21152) x = 7 (ISA bus in system, no VGA behind 21152) x = B (No ISA bus in system, VGA behind 21152) x = F (ISA bus in system, VGA behind 21152)
04h	Primary status/ command	FFFF01xyh	Clear status bits. x = 4 (No VGA snoop mode) x = 6 (VGA snoop mode) y = [0,5,6,7] ([configuration only, I/O only, memory only, all] enabled for downstream forwarding) <b>Write this register last.</b>

### 12.2 Enabling Timers and Setting Cache Line Size

Table 21 lists the accesses to enable the master latency timers, the target wait timers, and the burst count to desired values. The setting of cache line size is also shown.

**Table 21. Enabling Timers and Setting Cache Line Size**

Dword Offset	Register	Value	Notes
0Ch	Primary MLT/cache line size	0000xxyyh	xx = primary master latency timer value (low 3 bits = 0) yy = cache line size
18h	Secondary MLT/ subordinate/ secondary/primary bus numbers	wwxxyyzzh	ww = secondary master latency timer value (low 3 bits = 0) xx = subordinate bus number yy = secondary bus number zz = primary bus number





## ***Support, Products, and Documentation***

If you need technical support, a *Product Catalog*, or help deciding which documentation best meets your needs, visit the Intel World Wide Web Internet site:

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